AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS

1. (Currently Amended) A semiconductor device for use in a memory cell, comprising:

an active matrix provided with a semiconductor substrate, a transistor formed on the semiconductor substrate, an isolation region for isolating the transistor and a first insulating layer formed on top of the transistor and the isolation region;

a capacitor structure, formed on top of the first insulating layer, composed of a bottom electrode, a capacitor thin film placed on top of the bottom electrode and a top electrode formed on top of the capacitor thin film;

a second insulating layer formed on top of the transistor and the capacitor structure;

a metal interconnection formed on top of the second insulating layer to electrically connect the transistor for the capacitor structure;

a barrier layer formed on top of the metal interconnection; ~~and~~

an inter-metal dielectric (IMD) layer formed on top of the barrier layer by using a plasma chemical vapor deposition (CVD) in a hydrogen rich atmosphere, wherein the barrier layer is used for preventing the capacitor structure from the hydrogen;

a metal line formed on top of the IMD layer;

an additional barrier layer formed on top of the metal line; and

a passivation layer formed on top of the additional barrier layer by using a plasma CVD in a hydrogen rich atmosphere, wherein the additional barrier layer is used for preventing the capacitor structure from the hydrogen.

2. (Original) The semiconductor device of claim 1, wherein the capacitor thin film is made of a ferroelectric material selected from a group consisting of SBT (SrBiTaOx), PZT (PbZrTiOx) or the like.

3. (Currently Amended) The semiconductor device of claim 2, wherein the IMD layer is made of ~~a~~ an oxide material ~~such as SiO_2~~.

4. (Original) The semiconductor device of claim 3, wherein the plasma CVD is carried out at a low temperature by using silane (SiH_4) as a source gas.

5. (Currently Amended) The semiconductor device of claim 1, wherein the barrier layer is made of ~~a~~ an aluminum material ~~such as Al_2O_3~~.

6. (Original) The semiconductor device of claim 1, wherein the barrier layer has a thickness ranging from approximately 50 Å to approximately 150 Å.

7. (Original) The semiconductor device of claim 6, wherein the barrier layer is formed by using an atomic layer deposition (ALD) method.

8. (Original) The semiconductor device fo claim 7, wherein the ALD method is carried out by using trimethyl aluminum (TMA) and H_2O as a source gas and using N_2 as a purge gas.

9. (Cancelled)

10. (Currently Amended) The semiconductor device of claim ~~9~~ 1, wherein the additional barrier layer is made of ~~a~~ an aluminum material ~~such as Al_2O_3~~.

11. (Original) The semiconductor device of claim 10, wherein the additional barrier layer is formed by using an ALD method.